CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Currently Amended) A method comprising:

sending a first encrypted routine of a software driver from a processor to a graphics chip, wherein the software driver is to interface with the graphics chip, and where the first encrypted routine is an encrypted version of an encryption routine;

decrypting, at the graphics chip, the first encrypted routine to generate a plaintext routine, wherein the plaintext routine is a version of the encryption routine; and

storing the plaintext routine in memory in a location known to the software driver.

18. (Previously Presented) The method of claim 17, further including sending a decryption code to the graphics chip, where the decryption code is to be used by the graphics chip to decrypt the first encrypted routine.

19. (Previously Presented) The method of claim 17, wherein decrypting is performed by a 3D pipe of the graphics chip.

20. (Previously Presented) The method of claim 17, wherein decrypting is performed by a IDCT component of the graphics chip.

21. (Previously Presented) The method of claim 17, wherein decrypting is performed by dedicated encryption hardware of the graphics chip.

22. (Previously Presented) The method as in claim 17, wherein decrypting is performed through a series of components coupled within the graphics chip.

23. (Previously Presented) The method of claim 17, further including removing the plaintext routine.

24. (Previously Presented) The method of claim 17, further including:

encrypting, at the graphics chip, the plaintext routine to generate a second encrypted routine; and

storing the second encrypted routine in memory in a location known to the software driver.

25. (Previously Presented) The method of claim 24, further including sending an encryption code to the graphics chip, where the encryption code is to be used by the graphics chip to encrypt the plaintext routine.

26. (Original) The method of claim 24, wherein the second encrypted routine is a modified version of the first encrypted routine.

27. (Previously Presented) The method of claim 17, further including selecting the first encrypted routine from a plurality of different encrypted routines, wherein the plurality of different encrypted routines are functionally equivalent.

28. (Previously Presented) The method of claim 17, wherein decrypting includes using a map as a decryption key.

29. (Original) The method of claim 28, wherein the map includes a texture map.

30. (Previously Presented) The method of claim 17, wherein providing includes storing the plaintext routine in a location in memory accessible by the software driver, and where the location in memory is known to the software driver.

31. (Currently Amended) A system comprising:

a processor;

memory operably coupled to said processor;

a ~~peripheral device~~graphics chip, said ~~peripheral device~~graphics chip to decrypt a first encrypted routine, [[and]]generate a plaintext routine, and store the generated plaintext routine to a memory location of the memory;

a software driver, wherein said software driver is to interface with said ~~peripheral device~~graphics chip, said software driver including a program of instructions capable of being stored in said memory and executed by said processor, and wherein the memory location is known to the software driver, said program of instructions to manipulate said processor to:

send the first encrypted routine of said software driver to said peripheral device, wherein the first encrypted routine is an encrypted version of an encryption routine; and

execute the plaintext routine.

32. (Currently Amended) The system of claim 31, wherein the ~~peripheral device~~graphics chip includes a hardware component to encrypt the plaintext routine to generate a second encrypted routine, and where the second encrypted routine is a modified version of the first encrypted routine.

33. (Currently Amended) The system of claim 31, wherein the ~~peripheral device~~graphics chip includes a hardware component to decrypt the first encrypted routine to generate the plaintext routine.

34. (Canceled)

35. (Original) The system of claim 33, wherein the hardware component is a 3D pipe.

36. (Original) The system of claim 33, wherein the hardware component is a IDCT component.

37. (Original) The system of claim 33, wherein the hardware component is a dedicated hardware component.

38. (Currently Amended) The system of claim 31, wherein said program of instructions further include instructions to manipulate said processor to send a decryption code to said ~~peripheral device~~graphics chip, where the decryption code is to be used by said ~~peripheral device~~graphics chip to decrypt the first encrypted routine.

39. (Currently Amended) The system of claim 31, wherein said program of instructions further include instructions to manipulate said processor to send an encryption code to said ~~peripheral device~~graphics chip, where the encryption code is to be used by said ~~peripheral device~~graphics chip to encrypt the plaintext routine.

40. (Canceled)

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